IN THE SPECIFICATION:

Please insert the following section on page 1, after line 10:

-- **CROSS-REFERENCE TO RELATED APPLICATIONS**

This application claims the benefit of U.S. provisional patent application No. 60/165,013, filed on November 12, 1999, which is hereby incorporated herein by reference in its entirety.--

On page 3, please replace the second paragraph, lines 9-25, with the following paragraph:

--Stresses and strain gradients can limit the performance of both integrated and passive electrostatic MEMS devices. If the in-plane residual stress in doubly supported structures, for example, is too large, the structures may buckle. Conversely, if the stresses are too large the mechanical stiffness may be too large for the intended application. Stress control in sputtered structures has been achieved previously with high temperature anneals as is described, for example, in T. Abe and M. L. Reed, "Low Strain Sputtered Polysilicon for Micromechanical Structures," Proc. of Ninth International Workshop on Micro Electro-Mechanical Systems, San Diego Feb., 1996, pp. 258-262. These high temperature anneals (>1000°C) exceed their thermal annealing budget critical thermal budgets of integrated circuitry. The critical thermal budget is the budget beyond which the configuration of the integrated circuitry becomes permanently changed.--

On page 4, please replace the first paragraph, lines 1-21, with the following:

--forming clusters on top of the sacrificial layer before reaching a closing thickness at which the sputtered silicon

clusters have laterally extended and sufficiently overlapped to form a solid layer. The closing thickness is within several 100 Angstroms. The sputtered silicon within that closing thickness has a specific internal stress that differs significantly from the internal stress of the silicon deposited above the closing thickness. The phenomenon of the differing internal stress within the closing thickness is known to those skilled in the art as coalescence. The closing thickness is highly constant and introduces an essentially constant coalescence strain to the final structure. With increasing overall thickness of the micro-machined structure the influence of the coalescence strain becomes less influential. Depending upon the application, several additional properties may be important for the structural layer of a micro-fabricated device. Among these characteristics are film density, surface roughness and electrical resistivity, and permeability.--

On page 6, please replace the first paragraph under "SUMMARY", lines 9-16, with the following paragraph:

--A sputtered layer is introduced. The sputtered layer, preferably from silicon, is deposited with predetermined sputtering criteria resulting in a predetermined pre-annealing configuration. This pre-annealing configuration is transformed during a low temperature annealing process into a post-annealing configuration. A released structure is micro-machined from the sputtered layer in its post-annealed configuration.--

On page 6, please replace the bottom paragraph, lines 26-32, with the following paragraph:

--The released structure has a resulting in-plane strain and a resulting strain gradient, which are predetermined in accordance with deformation configurations of the released structure. The deformation configuration depends on the shape of the released structure and on the fashion it is supported. The deformation configurations are distinguished between an essentially buckling-free deformation--

On page 8, please replace the second paragraph, lines 5-15, with the following paragraph:

--For buckling-influenced deformation configurations, second sputtering criteria predominantly include and sacrificial layer material are defined such that the sputtered layer has a predetermined resulting or initial in-plane strain. Sputtering power, ambient sputtering pressure and sputtering temperature are selected from a zone-T of the Thornton zone diagram as known to those skilled in the art. In the case, where a low temperature annealing is included in the fabrication process, the second sputtering criteria are selected in correlation with the annealing transformation.--

On page 9, please replace the second paragraph, lines 14-26, with the following paragraph:

--The sputtered layer made from silicon is porous and permeable to HF-based etches at approximately ten times the thicknesses reported for LPCVD deposited polysilicon. The initial porosity remains mostly unaltered during the annealing process such that encapsulated cavities with relatively thick cover layers may be fabricated compared to

those made from polysilicon. Consequently, larger and/or more solid cover layers may be fabricated compared to those from prior art methods. The cover layers are stiffer and better able to withstand the capillary forces of the wet etch in the encapsulated cavity beneath the silicon during a drying process. The annealing need not be performed prior to the release etching.--

On page 12, please replace the bottom paragraph, lines 19-32, with the following paragraph:

--The sputtering process **Sp** is either defined by first sputtering criteria **P1** or by second sputtering criteria **P2**. The first sputtering criteria **P1** provide an initial sputtered layer **3A** having a first pre-annealing configuration including a predetermined initial strain gradient. The second set of sputtering criteria provides the initial sputtered layer 3A having a second pre-annealing configuration including a predetermined initial in-plane strain. The sputtering process should be of zone-T type to ensure that low stresses are achieved. The deposition temperature should thus be approximately between room temperature and 200°C. An Ar working gas deposition pressure ranging from 8 to 14 mTorr yielded acceptable stresses. Films deposited at 8 mTorr were more dense. Those--

On page 13, please replace the bottom paragraph, lines 11-29, with the following paragraph:

--**Fig. 2** shows a simplified section of the work piece of **Fig. 1** during the annealing process. The simplified section of **Fig. 2** features optional aluminum terminals **Al**, which may be

deposited after the deposition of the initial sputtered layer **3A** and before the work piece is exposed to a low temperature annealing process **TAn** indicating in **Fig. 2** a rectangle labeled **TB** for a thermal annealing budget **TB** induced on the work piece during the low temperature annealing process **TAn.** The definition of the thermal annealing budget **TB** includes a maximum annealing temperature and an annealing duration. The thermal annealing budget **TB** is smaller than the critical thermal budget of eventual electronic circuitry of the work piece simultaneously exposed to the low temperature annealing process **TAn.** The films were annealed in nitrogen and a nitrogen-hydrogen environment at temperatures at or below 350°C. The films annealed in the nitrogen-hydrogen environment showed a marked decrease in conductivity and a decrease in the strain gradient.--